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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,735	12/20/2005	Jan Dikken	GB30100US1	7773

65913 7590 03/20/2008

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EXAMINER	
NGUYEN, MATTHEW VAN	
ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
03/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,735	DIKKEN ET AL.	
	Examiner	Art Unit	
	MATTHEW V. NGUYEN	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-16 and 18* is/are rejected.

7)☒ Claim(s) *9 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The disclosure should be carefully reviewed and ensure that any and all grammatical, idiomatic, and spelling or other minor errors are corrected. For instance, in claim 2, line 5, "betwl8en" is a spelling error.

2. The abstract of the disclosure is objected to because it should be written in a separate page and contains no reference numbers. Correction is required. See MPEP § 608.01(b).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10-16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by FR 2 680 056 (hereinafter '056).

With regard to claims 1-8, 10-16 and 18, '056 (i.e., Figs. 1, 5, 6) shows a switching circuit and a method thereof having a first field effect transistor (K1, or MOS1 in Fig. 6) and a second field effect transistor (K2, or MOS2 in Fig. 6) connected in series between an input terminal (upper terminal of E) and a ground terminal (lower terminal of E), wherein a source of the first transistor is connected to the drain of the second transistor and a source of the second transistor is connected to the ground terminals, the circuit comprising: control means (i.e., AD1, AD2 …) for driving the first and second transistors alternately such that there is a dead time period during which both transistors

are off; and means (i.e., RET1, RET2 …) for adjusting the length of the dead time period according to a voltage difference between the drain and the source of the first or second transistor; the first and/or the second transistors are constructed on an integrated circuit die, each of said transistors having respective drain and source regions on said die, further comprising sensing means (V1) for sensing the voltaglage difference betweeen the drain and the source of the first transistor (K1), wherein this sensing means has a first connection, which is directly connected to the source region of the first transistor (K1), the first and/or second connections are Kelvin connections, the sensing means (V1, V2) senses the voltage difference during the dead time period; the adjusting means (RET1, RET2) adjusts the length of future dead time periods according to the voltage difference during the dead time period and to the length of time that the voltage difference exceeds a threshold voltage; the adjusting means adjusts the length of the dead time period according to the length of time, and to the magnitude that the voltage difference exceeds a threshold voltage; and the length of the dead time period is linearly dependent on the length of time for which the voltage difference exceeds a threshold value (i.e., Fig. 5).

5. Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sauerlander et al. (U.S. pat. No. 6,381,160).

With regard to claims 1 and 14, Sauerlander et al. (i.e., Fig. 2) shows a switching circuit and a method thereof having a first field effect transistor (S1, col. 3, line 34)) and a second field effect transistor (S2) connected in series between an input terminal

(upper terminal of U1) and a ground terminal (lower terminal of U2), wherein a source of the first transistor is connected to the drain of the second transistor and a source of the second transistor is connected to the ground terminals, the circuit comprising: control means (i.e., 10, 10' …) for driving the first and second transistors alternately such that there is a dead time period during which both transistors are off; and means (i.e., Fig. 3, col. 4, lines 32-33) for adjusting the length of the dead time period according to a voltage difference between the drain and the source of the first or second transistor.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6-8 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticpated by Umemoto et al. (US Pat. No. 2003/0231011) .

With regard to claims 1, 6-8 and 11-14, Umemoto et al. (i.e., Fig. 1) shows a switching circuit and a method thereof having a first field effect transistor (N1) and a second field effect transistor (N2) connected in series between an input terminal (Vin) and a ground terminal (GND), wherein a source of the first transistor is connected to the drain of the second transistor and a source of the second transistor is connected to the ground terminals, the circuit comprising: control means (i.e., SR1, SR2 …) for driving the first and second transistors alternately such that there is a dead time period during which both transistors are off; and means (i.e., OSV1 …, Fig. 2A, 2B, [0032]) for adjusting the length of the dead time period according to a voltage difference between

the drain and the source of the first or second transistor; the adjusting means adjusts the length of future dead time periods according to the voltage difference during the dead time period; or according to the length of time and the magnitude that the voltage difference exceeds a threshold voltage (i.e., Fig. 2A, 2B).

7. Claims 9 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of prior art of record taken alone or in combination shows the adjusting means adjusts the length of the dead time period such that the length of the dead time period is exponentially dependent on the magnitude by which threshold voltage difference exceeds the threshold voltage as recited in claims 9 and 17.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Massie et al. (U.S. Pat. No. 5,777,461), Dequina et al. (U.S. Pat. No. 6,940,262) and Yoshihawa (U.S. Pat. No. 7,294,992) also disclose switching circuits each of which comprising first and second field effect transistors connected in series between an input terminal and a ground terminal, and a control circuit for driving the first and second transistors alternately such that there is a dead time period during which both transistors are off.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW V. NGUYEN whose telephone number is (571)272-2081. The examiner can normally be reached on 8 HOURS M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AKM ULLAH can be reached on (571)272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MATTHEW V NGUYEN/
Primary Examiner, Art Unit 2838